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EXAMINER	
JANAKIRAMAN, NITHYA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,032	NIGHTINGALE ET AL.	
	Examiner	Art Unit	
	Nithya Janakiraman	2123	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the application filed on 7/21/2004. Claims 1-46 are presented for examination.

Drawings

1. The drawings are objected to because of the following informalities: Figures 1-5D do not conform to 37 CFR 1.84(g), (l), and (p). See Draftsperson's Patent Drawing Review. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The abstract of the disclosure is objected to because it contains greater than 150 words. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 1-46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4. Claim 1 concludes with "generating revised timing information". The mere generation of data does not constitute statutory subject matter, as there is no recited practical application. Claim 12 is rejected under similar rationale. All depending claims are rejected as well.

5. Claim 29 recites a "system for simulating" containing a "master logic unit software model", a "slave logic unit model", and a "bus software model". Giving the claim a broad reasonable interpretation, these limitations are broad enough to encompass a software "system" with software components. Claim 29 is therefore held as software *per se*. All depending claims are rejected as well.

6. Claim 46 recites a "computer program" containing a "master logic unit software model", a "slave logic unit model", and a "bus software model". Giving the claim a broad reasonable interpretation, these limitations are broad enough to encompass a software "system" with software components. Claim 46 is therefore held as software *per se*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Publication 2002/0163932, Fischer (hereinafter Fischer) in view of US Patent 6,393,500, Thekkath (hereinafter Thekkath).

8. Fischer discloses a method for transaction between a master device and a slave device, and continuously generating revised timing information for the data transactions over the network (see Abstract). However, Fischer does not simulate the transaction, nor does Fischer compensate for two or more concurrent transactions.

9. Thekkath discloses determining whether two or more data transfers occur over a bus, and provides for precluding bus contentions (see column 6, lines 57-67 and column 7, lines 1-5), as well as for simulating the bus/master device.

10. Fischer and Thekkath are analogous art because they are both related to the field of data transfers over a bus.

11. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the simulation of Thekkath with the bus transactions of Fischer because it is desirable to test and simulate for "a burst data transaction to be optimized...for efficient transfer over a bus" (see Thekkath, column 6, lines 14-25). It would also have been obvious to one having ordinary skill in the art at the time the invention was made

to combine the provisions for bus contention of Thekkath with the method of transferring data over a bus of Fischer, because "If two devices were to execute a data transfer at the same time, then signals on the bus would be corrupted, thus precluding any transfer of data" (see Thekkath, column 1, lines 62-67), which is clearly undesirable to one of ordinary skill in the art.

12. Regarding claim 1, Fischer and Thekkath teach:

A method of simulating the operation of a data processing apparatus *(Thekkath, column 5, lines 29-37)* to determine timing information of data transfers, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus *(Fischer, paragraph [0012], "master node", "slave node"*), the method comprising the steps of:

a) generating anticipated timing information for each successive data transfer over the bus by assuming that each successive data transfer can occur with exclusive access to the bus *(Fischer teaches that timing information is determined for each data transfer in paragraph [0012], "Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times")*;

b) determining whether the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus *(Thekkath teaches that transaction interference on a bus would be avoided by detecting what would be the capability of a bus and adjusting accordingly using arbitration logic, column 5, lines 1-10, "The transaction control logic varies burst width*

according to the burst transaction capability"; column 7, lines 1-5, "...preclude bus contentions and to provide fair and timely access to the bus for all initiating devices"); and

c) in the event that the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus *(Thekkath teaches the detection of transaction interference in column 7, lines 1-5, using arbitration logic)*, generating revised timing information for those data transfers, the revised timing information being generated using bus status information until those data transfers have been completed *(Fischer teaches that continuous revisions take place to adjust for the transaction interference, or errors, of Thekkath in paragraph [0012], "Each slave node clock is continuously corrected compared with the master node clock to smooth slave clock error to an average of zero compared with the master clock as a reference in response to a message from the master node...Packets at slave nodes are then transmitted according to the determined future best packet assembly time information").*

13. Regarding claim 2, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein the step a) further comprises the step of generating anticipated timing information for each successive data transfer between one master logic unit and one slave logic unit over the bus to which that master logic unit and that slave logic unit have exclusive access *(Fischer, paragraph [0012], "Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times").*

14. Regarding claim 3, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein the anticipated timing information comprises a data transfer window indicative of the time during which that data transfer will occur over the bus *(Fischer, paragraph [0012], "Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times").*

15. Regarding claim 4, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein the anticipated timing information comprises data transfer commencement information indicative of the time at which that data transfer will commence on the bus and data transfer completion information indicative of the time at which that data transfer will complete on the bus *(Fischer, paragraph [0012], "Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times").*

16. Regarding claim 5, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein each data transfer comprises the transfer of a number of data values over the bus and the anticipated timing information comprises data value transfer information indicative of the time at which each data value will be transferred over the bus *(Fischer, paragraph [0012], "A best arrival time for the reception by the master node of each particular packet transmitted by each particular slave node is determined at the master node").*

17. Regarding claim 6, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein the step b) further comprises the step of comparing the anticipated timing information for each successive data transfer to determine whether two or more concurrent data transfers would occur on the bus *(Thekkath, column 7, lines 1-5)*.

18. Regarding claim 7, Fischer and Thekkath teach:

The method as claimed in claim 6, wherein the step b) further comprises the step of determining whether two or more concurrent data transfers would occur on the bus by determining whether the anticipated timing information indicates that one data transfer will not complete prior to another data transfer commencing *(Thekkath, column 7, lines 1-5)*.

19. Regarding claim 8, Fischer and Thekkath teach:

The method as claimed in claim 1, wherein the step c) further comprises the step of generating bus status information indicative of the status of the bus during at least a period when the anticipated timing information indicates that two or more concurrent data transfers would occur on the bus *(Thekkath, column 7, lines 1-5)*.

20. Regarding claim 9, Fischer and Thekkath teach:

The method as claimed in claim 8, wherein the bus status information includes information indicative of which master logic unit/slave logic unit pair have access to the bus at any point in time during at least the period *(Fischer, paragraph [0055])*.

21. Regarding claim 10, Fischer and Thekkath teach:

The method as claimed in claim 8, wherein the step c) further comprises the step determining from the generating bus status information which of those data transfers will occur on the bus at any point in time during at least the period *(Fischer, paragraph [0055])*.

22. Regarding claim 11, Fischer and Thekkath teach:

The method as claimed in claim 9, wherein the step c) further comprises the step of generating revised timing information indicative of the time during which each of those data transfers occur over the bus *(Fischer, paragraph [0012], Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times")*.

23. Regarding claim 12 (29 and 46), Fischer and Thekkath teach:

A method of simulating the operation of a data processing apparatus *(Thekkath, column 5, lines 29-37)* using a software model to determine timing information of data transfers *(Fischer, paragraph [0493], "The simulation models a master clock jitter...")*, the data processing apparatus comprising a number of master logic units and slave logic units coupled via a bus, the data processing apparatus being operable to perform the data transfers between the master logic units and the slave logic units over the bus *(Fischer, paragraph [0012], "master node", "slave node")*, the method comprising the steps of:

a) in response to an indication that a data transfer is to occur, generating data transfer information indicative of the data transfer using a master logic unit model and a slave logic unit model *(paragraph [0012], "Best arrival times for packets transmitted from slave nodes to the master node are communicated from the master node to the slave nodes");*

b) generating anticipated timing information from the data transfer information using the master logic unit model and the slave logic unit model, the anticipated timing information being generated by assuming that the data transfer will occur with exclusive access to the bus *(Fischer teaches that timing information is determined for each data transfer in paragraph [0012], "Best packet assembly times for packets to be transmitted by the particular slave node to the master node in the future in order for the packets to be received by the master node at future master clock referenced best arrival times")*;

c) determining from the anticipated timing information whether two or more concurrent data transfers will occur on the bus *(Thekkath teaches that transaction interference on a bus would be avoided by detecting what would be the capability of a bus and adjusting accordingly using arbitration logic, column 5, lines 1-10, "The transaction control logic varies burst width according to the burst transaction capability"; column 7, lines 1-5, "...preclude bus contentions and to provide fair and timely access to the bus for all initiating devices")*; and

d) in the event that is it anticipated that two or more concurrent data transfers will occur on the bus *(Thekkath teaches the detection of transaction interference in column 7, lines 1-5, using arbitration logic)*, generating revised timing information for those data transfers using the master logic unit model and the slave logic unit model, the revised timing information being generated by modelling the status of the bus during at least the period when it is anticipated that two or

more concurrent data transfers will occur *(Fischer teaches that continuous revisions take place to adjust for the transaction interference, or errors, of Thekkath in paragraph [0012], "Each slave node clock is continuously corrected compared with the master node clock to smooth slave clock error to an average of zero compared with the master clock as a reference in response to a message from the master node...Packets at slave nodes are then transmitted according to the determined future best packet assembly time information").*

24. Regarding claim 13 (and 30), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein the data transfer information includes information indicative of the type and size of data transfer *(Fischer, paragraph [0009]).*

25. Regarding claim 14 (and 31), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein the step b) comprises generating anticipated timing information comprising timing values generated by the master logic unit model and the slave logic unit model indicative of the time during which that data transfer will occur over the bus *(Fischer, paragraph [0012], "Best arrival times for packets transmitted from slave nodes to the master node are communicated from the master node to the slave nodes").*

26. Regarding claim 15 (and 32), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein the step b) comprises generating anticipated timing information comprising data transfer commencement information using the master logic unit model, the data transfer commencement information being indicative of the time at which that

data transfer will commence on the bus and generating data transfer completion information using the slave logic unit model, the data transfer completion information being indicative of the time at which that data transfer will complete on the bus *(Fischer, paragraph [0012], "Packets at slave nodes are then transmitted according to the determined future best packet assembly time information").*

27. Regarding claim 16 (and 33), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein each data transfer comprises the transfer of a number of data values over the bus and the step b) comprises generating anticipated timing information comprising data value transfer information indicative of the time at which each data value will be transferred over the bus *(Fischer, paragraph [0012], "Best arrival times for packets transmitted from slave nodes to the master node are communicated from the master node to the slave nodes").*

28. Regarding claim 17 (and 34), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein the step c) further comprises the step of comparing the anticipated timing information for each successive data transfer using a arbiter model to determine whether two or more concurrent data transfers would occur on the bus *(Thekkath, column 7, lines 1-5)..*

29. Regarding claim 18 (and 35), Fischer and Thekkath teach:

The method as claimed in claim 17, wherein the step c) further comprises the step of determining whether two or more concurrent data transfers would occur on the bus by determining whether the anticipated timing information indicates that one data transfer will not complete prior to another data transfer commencing *(Thekkath, column 7, lines 1-5)*..

30. Regarding claim 19 (and 36), Fischer and Thekkath teach:

The method as claimed in claim 12, further comprising the step of: generating a transaction including the data transfer information *(Fischer, paragraph [0012])*.

31. Regarding claim 20 (and 37), Fischer and Thekkath teach:

The method as claimed in claim 19, wherein the steps a) and b) comprise the steps of:

generating master data transfer information and master anticipated timing information from the data transfer information using a master logic unit model;

storing the master data transfer information and the master anticipated timing information in the transaction;

passing the transaction to the slave logic unit model;

generating slave data transfer information and slave anticipated timing information from the data transfer information using a slave logic unit model; and

storing the slave data transfer information and the slave anticipated timing information in the transaction *(Fischer, paragraph [0012])*.

32. Regarding claim 21 (and 38), Fischer and Thekkath teach:

The method as claimed in claim 19, wherein the step c) further comprises the steps of: passing the transaction to an arbiter model; updating a bus allocation table with the anticipated timing information in the transaction *(Fischer, paragraph [0012])*; determining from the bus allocation table whether two or more concurrent data transfers are anticipated to occur *(Thekkath, column 7, lines 1-5)*.

33. Regarding claim 22 (and 39), Fischer and Thekkath teach:

The method as claimed in claim 19, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of: causing each master logic unit model and slave logic unit model associated with the two or more concurrent data transfers to initialise timing models operable to simulate bus signals generated by each of the corresponding master logic units and slave logic units on a clock cycle by clock cycle basis *(Fischer, paragraph [0012])*.

34. Regarding claim 23 (and 40), Fischer and Thekkath teach:

The method as claimed in claim 22, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the steps of:

setting a current clock cycle from which the bus signals are to be simulated;

initialising the timing models based on the current clock cycle and using anticipated timing information within the transactions associated with the two or more concurrent data transfers *(Fischer, paragraph [0012])*.

35. Regarding claim 24 (and 41), Fischer and Thekkath teach:

The method as claimed in claim 22, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of: determining, using an arbiter model and based on the simulated bus signals, which of the master logic unit models and slave logic unit models will be allocated access to the bus during any particular clock cycle *(Fischer, paragraph [0012])*.

36. Regarding claim 25 (and 42), Fischer and Thekkath teach:

The method as claimed in claim 24, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of: signalling the master logic unit models and slave logic unit models with the outcome of the determination *(Fischer, paragraph [0012])*.

37. Regarding claim 26 (and 43), Fischer and Thekkath teach:

The method as claimed in claim 25, wherein in the event that is it anticipated that two or more concurrent data transfers will occur the step d) further comprises the step of: on receipt of a signal indicating to a master logic unit model or slave logic unit model that access to the bus has been granted, generating the revised timing information indicative of the actual clock cycles over which the data transfer occurred *(Fischer, paragraph [0012])*.

38. Regarding claim 27 (and 44), Fischer and Thekkath teach:

The method as claimed in claim 22, wherein once the revised timing information has been generated for two or more concurrent data transfers, simulating bus signals generated by each of the corresponding master logic units and slave logic units on a clock cycle by clock cycle basis is suspended *(Fischer, paragraph [0012])*.

39. Regarding claim 28 (and 45), Fischer and Thekkath teach:

The method as claimed in claim 12, wherein in the event that is it anticipated that two or more concurrent data transfers will not occur, the step d) further comprises the step of: causing the associated master logic unit model and slave logic unit model to remain inactive for the period of the data transfer *(Fischer, paragraph [0508])*.

Additional References

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

41. US Publication 2005/0131666: a circuit simulator produces a dump file containing a set of waveform data sequences, each corresponding to a separate signal within the circuit, and representing states of its corresponding signal at a succession of times during the circuit simulation. Based on a mapping of the waveform data sequences to lines of a bus, and on transaction data models describing characteristic signal patterns appearing on the bus during each type of transaction that can occur on the bus, a transaction analysis system identifies transactions that occurred on the bus during the simulation.

42. US Patent 6,490,642: An apparatus is presented for improving the efficiency of data transfers between devices interconnected over an on-chip system bus a multi-master computer system configuration. Bus efficiency is improved by providing an apparatus for controlling a read-modify-write transaction to an address in a bus slave device that does not suspend essential features of the system bus during the transaction, namely, pipelining and transaction splitting.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nithya Janakiraman whose telephone number is 571-270-1003. The examiner can normally be reached on Monday-Thursday, 8:00am-5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on (571)272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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